Abstract of the Disclosure

An EEPROM device and a method of fabricating same. In one aspect, an EEPROM device comprises: a memory transistor including a tunnel insulating layer, first conductive layer patterns, and second conductive layer patterns stacked on a first portion of a semiconductor substrate, and common source regions and floating junction regions arranged at opposite sides of the second conductive layer patterns; and a selection transistor, which is connected to the floating junction regions, and includes a gate insulating layer, the first conductive layer patterns, and the second conductive layer patterns stacked on a second portion of the semiconductor substrate, and drain regions arranged at one side of the second conductive layer patterns opposite the floating junction regions. The first conductive layer patterns in the memory transistor are separated by cell unit and floated, and the insulating layer and the second conductive layer patterns stacked on the first conductive layer patterns are connected to a cell and an adjacent cell, and the first conductive layer patterns and the second conductive layer patterns of the selection transistor are etched and connected by metal plugs. The EEPROM is fabricated using a simplified process which combines a floating gate mask and ion implantation mask into one mask, and which provides reduced resistance by connecting word lines using the metal plugs.